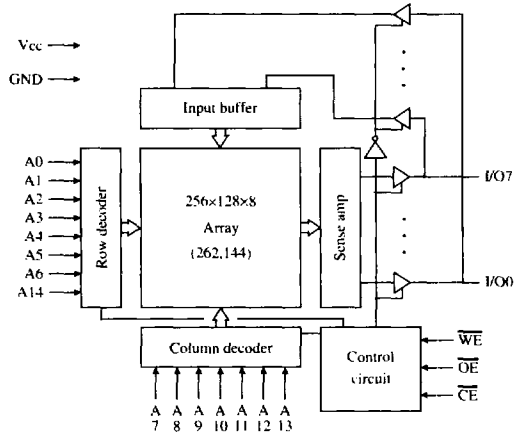
SRAM

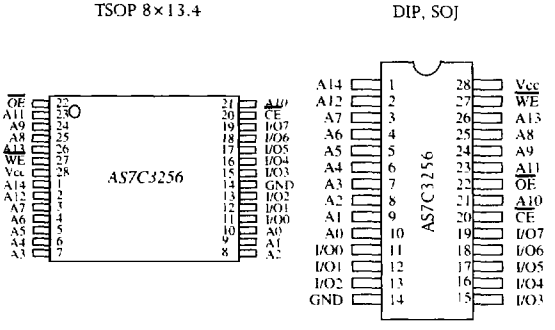
Features

- Organization: 32,768 words × 8 bits
- Single 3.3 ± 0.3V power supply
- 5V tolerant I/O specification
- High speed
  - 10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Very low power consumption
  - Active: 216 mW max, 10 ns cycle
  - Standby: 3.6 mW max, CMOS I/O
    1.1 mW max, CMOS I/O, L version
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- Ideal for cache, modem, portable computing
  - 75% power reduction during CPU idle mode
- 28-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
  - 8 × 13.4 TSOP
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

		7C3256-12	7C3256-15	7C3256-20	Unit
Maximum address access time		12	15	20	ns
Maximum output enable access time		3	4	5	ns
Maximum operating current		55	50	45	mA
Maximum CMOS standby current		1.0	1.0	1.0	mA
	L	0.3	0.3	0.3	mA

Shaded areas contain advance information.

Functional description

The AS7C3256 is a 3.3V high performance CMOS 262,144-bit Static Random-Access Memory (SRAM) organized as 32,768 words × 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters standby mode when $\overline{CE}$ is HIGH. CMOS standby mode consumes ≤3.6 mW (≤1.1 mW for the L version). Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode. Both versions of the AS7C3256 offer 2.0V data retention.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 3/3/4/5 ns are ideal for high performance applications. The chip enable ($\overline{CE}$) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is HIGH, or write enable is LOW, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible and 5V tolerant. Operation is from a single 3.3±0.3V supply. The AS7C3256 is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{CC}	−0.5	+4.6	V
Input voltage relative to GND	V_{IN}	−0.5	+6.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable
L	H	L	D_{out}	Read
L	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

(T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.0	–	5.5	V
	V_{IL}	−0.5†	–	0.8	V

†V_{IL} min = −2.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics [1]

(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test conditions		-10	-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}			–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ = V_{IH}, V_{CC} = Max, V_{out} = GND to V_{CC}			–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE}$ = V_{IL}, f = f_{max}, I_{out} = 0 mA			–	55	–	50	–	45	mA
Standby power supply current	I_{SB}	$\overline{CE}$ = V_{IH}, f = f_{max}			–	20	–	20	–	15	mA
	I_{SB1}	$\overline{CE}$ ≥ V_{CC}–0.2V, V_{in} ≤ 0.2V *or* V_{in} ≥ V_{CC}–0.2V, f = 0			–	1.0	–	1.0	–	1.0	mA
			L		–	0.3	–	0.3	–	0.3	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min			–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min			2.4	–	2.4	–	2.4	–	V

Shaded areas contain advance information

Capacitance [2]

(f = 1 MHz, T_a = Room temperature, V_{CC} = 3.3V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

SRAM

Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read cycle [3,9]

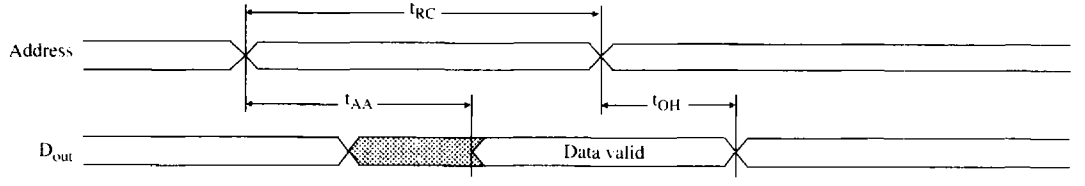
(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

		-10	-12		-15		-20			
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}		12	–	15	–	20	–	ns	
Address access time	t_{AA}		–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}		–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}		–	3	–	4	–	5	ns	
Output hold from address change	t_{OH}		3	–	3	–	3	–	ns	5
$\overline{CE}$ LOW to output in Low Z	t_{CLZ}		3	–	3	–	3	–	ns	4, 5
$\overline{CE}$ HIGH to output in High Z	t_{CHZ}		–	3	–	4	–	5	ns	4, 5
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}		0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}		–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}		0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}		–	12	–	15	–	20	ns	4, 5

Shaded areas contain advance information

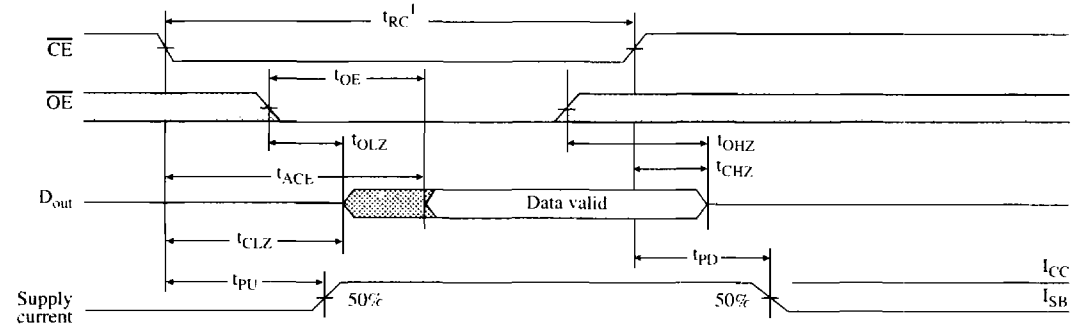
Read waveform 1 [3,6,7,9]

Address controlled



Read waveform 2 [3,6,8,9]

$\overline{CE}$ controlled



Write cycle [11]

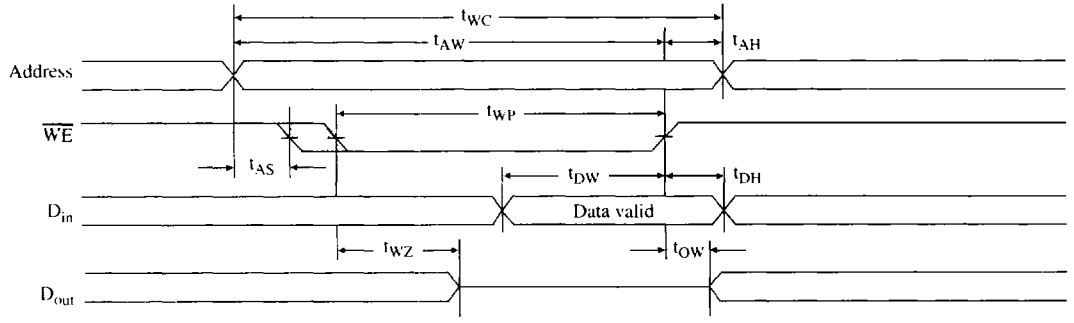
(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0 to +70°C)

		-10	-12		-15		-20			
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}		12	–	15	–	20	–	ns	
Chip enable to write end	t_{CW}		10	–	12	–	12	–	ns	
Address setup to write end	t_{AW}		10	–	12	–	12	–	ns	
Address setup time	t_{AS}		0	–	0	–	0	–	ns	
Write pulse width	t_{WP}		8	–	9	–	12	–	ns	
Address hold from end of write	t_{AH}		0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}		6	–	8	–	10	–	ns	
Data hold time	t_{DH}		0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}		–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}		3	–	3	–	3	–	ns	4, 5

Shaded areas contain advance information

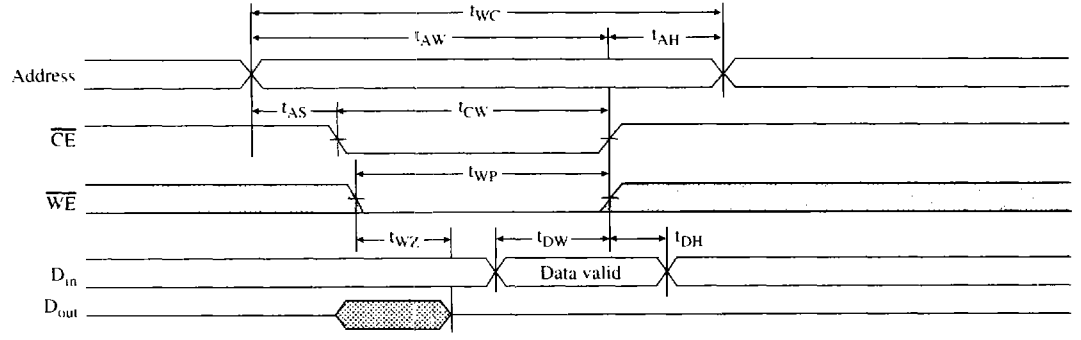
Write waveform 1 [10,11]

$\overline{WE}$ controlled



Write waveform 2 [10,11]

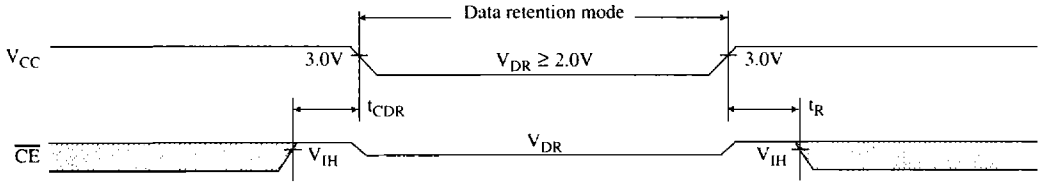
$\overline{CE}$ controlled



Data retention characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CC}-0.2V$	–	500	µA
			–	150 (L)	µA
Chip enable to data retention time	t_{CDR}	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

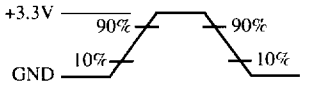


Figure A: Input waveform

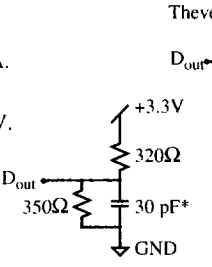


Figure B: Output load

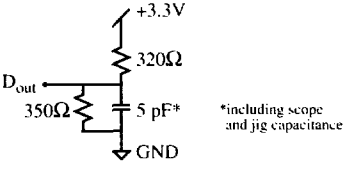


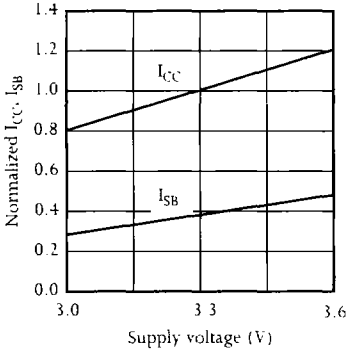
Figure C: Output load for t_{CLZ}, t_{CHZ}

Notes

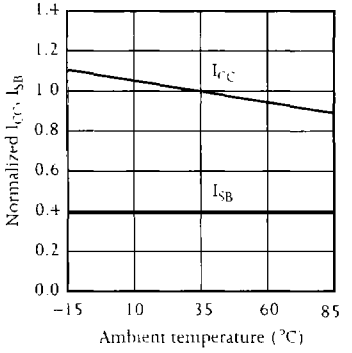
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.

Typical DC and AC characteristics

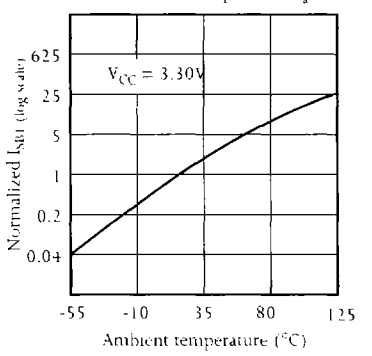
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



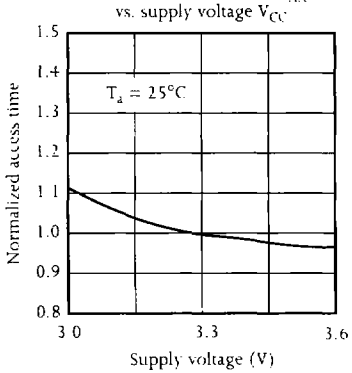
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



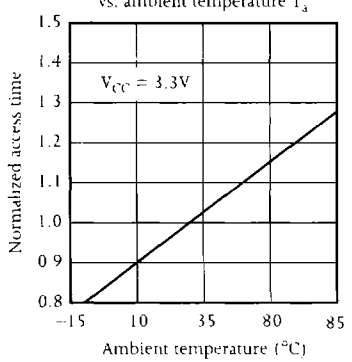
Normalized supply current I_{SB1} vs. ambient temperature T_a



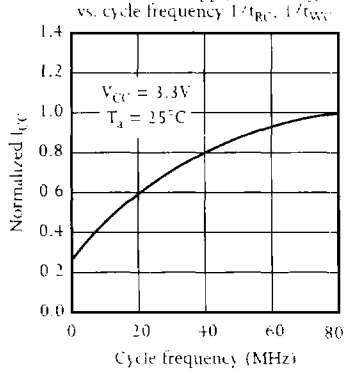
Normalized access time t_{AA} vs. supply voltage V_{CC}



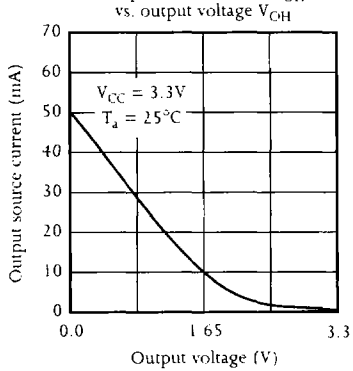
Normalized access time t_{AA} vs. ambient temperature T_a



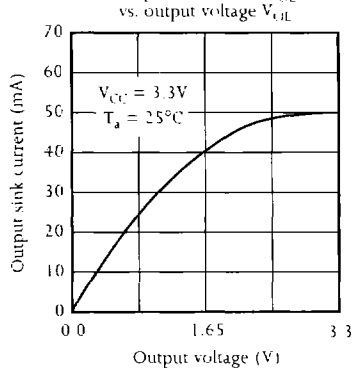
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



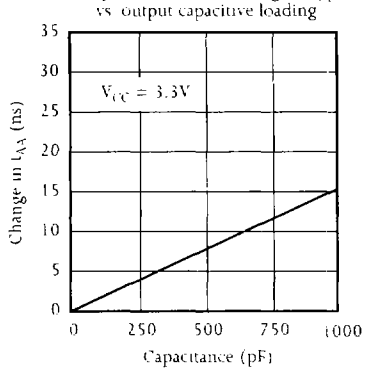
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



AS7C3256 ordering information

Package / Access time	10 ns	12 ns	15 ns	20 ns
Plastic DIP, 300 mil		AS7C3256-12PC AS7C3256L-12PC	AS7C3256-15PC AS7C3256L-15PC	AS7C3256-20PC AS7C3256L-20PC
Plastic SOJ, 300 mil		AS7C3256-12JC AS7C3256L-12JC	AS7C3256-15JC AS7C3256L-15JC	AS7C3256-20JC AS7C3256L-20JC
TSOP 8x13.4		AS7C3256-12TC AS7C3256L-12TC	AS7C3256-15TC AS7C3256L-15TC	AS7C3256-20TC AS7C3256L-20TC

Shaded areas contain advance information

AS7C3256 part numbering system

AS7C	3	256	–XX	X	C
SRAM prefix	Blank = 5V supply 3 = 3.3V supply	Device number	Access time	Package P = PDIP 300 mil J = SOJ 300 mil T = TSOP 8x13.4	Commercial temperature range, 0°C to 70 °C